REMARKS

The present application was filed on February 1, 2002 with claims 1-15. Claims 14 and 15 were withdrawn from consideration as a result of an election made in the Response to Restriction Requirement dated January 14, 2003. Claims 1-15 are currently pending in the present application. In the outstanding Office Action dated April 9, 2003, the Examiner has: (i) indicated that claims 14 and 15 are withdrawn from consideration as being drawn to a nonelected invention; (ii) acknowledged Applicant's election of claims 1-13 without traverse; (iii) objected to the abstract based on an informality; (iv) objected to the disclosure based on informalities; (v) objected to claims 2, 3, 7 and 8 based on informalities; (vi) rejected claims 3, 11 and 13 under 35 U.S.C. §112, second paragraph as being indefinite; (vii) rejected claims 1-4, 9, 12 and 13 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,955,775 to Miwa (hereinafter "Miwa"); (viii) rejected claim 6 under 35 U.S.C. §103(a) as being unpatentable over Miwa; (ix) rejected claim 10 under 35 U.S.C. §103(a) as being unpatentable over Miwa in view of U.S. Patent No. 5,885,880 to Gomi (hereinafter "Gomi"); and (x) indicated that claims 5, 7, 8 and 11 contain allowable subject matter.

In this response, the abstract has been amended in a manner which is believed to address the Examiner's objection to the abstract. Claims 2, 3 and 8 have been amended in a manner which is believed to address the Examiner's objections to these claims. Claims 14 and 15 have been canceled without prejudice, claims 1-3, 5, 7, 8, 11 and 13 have been amended (allowable claims 5, 7, 8 and 11 having been recast in independent form), and claims 16 and 17 have been added. Applicants respectfully request reconsideration of the present application in view of the above amendments and the following remarks.

With regard to the Examiner's objection to the disclosure, Applicant submits herewith a proposed red-lined drawing change to FIGS. 13 and 14 of the drawings. Specifically, with regard to FIG. 13, reference numerals 200, 300 and 302 have been changed to 1200, 1300 and 1302, respectively, and with regard to FIG. 14, reference numeral 400 has been changed to 1400. The drawing changes are intended to cure certain informalities in FIGS. 13 and 14 and thereby provide

proper correspondence with the disclosure. These changes are believed to address the Examiner's objection to the disclosure noted on page 2, paragraph 4 of the present Office Action. Approval of the drawing changes and withdrawal of the objection to the disclosure are respectfully requested.

Claims 3, 11 and 13 stand rejected under 35 U.S.C. §112, second paragraph as being indefinite. Specifically, with regard to claim 3, the Examiner contends that the phrase "etching the semiconductor wafer until the oxide layer on a horizontal portion of the semiconductor wafer is substantially removed" is unclear (present Office Action; page 3, first paragraph). With regard to claim 13, the Examiner contends that the phrase "predetermined characteristics" is unclear. Claims 3 and 13 have been amended in a manner which Applicant believes addresses the §112 rejections.

OK

With regard to claim 11, the Examiner contends that the phrase "forming a dielectric layer on the semiconductor wafer such that an upper surface of the semiconductor wafer is substantially planar is unclear (present Office Action; page 3, paragraph 2). Applicant respectfully traverses this rejection and submits that the semiconductor wafer is intended to comprise all of the layers (see, e.g., Specification, page 6, lines 9-10). An upper surface of the dielectric layer forms the upper surface of the wafer. Therefore, forming the dielectric layer on the semiconductor wafer such that the upper surface of the semiconductor wafer is substantially planar, as set forth in claim 11, is believed to be correct.

not OK

Claims 1-4, 9, 12 and 13 stand rejected under §102(b) as being anticipated by the Miwa reference. With regard to claim 1, the Examiner contends that Miwa discloses all of the elements of the claimed invention. In response, claim 1 has been amended to incorporate a feature of the invention recited in claims 5 and 7. Specifically, claim 1 has been amended to further define the invention such that the step of forming the first and second electrodes further comprises rapid thermal annealing the semiconductor wafer for substantially removing residual oxide between the first polysilicon layer and the upper surface of the semiconductor wafer and/or the step of forming the third and fourth electrodes further comprises rapid thermal annealing the semiconductor wafer for substantially removing residual oxide between the second polysilicon layer and the upper surface

not OK, limitation of claim 4 is missing

of the semiconductor wafer. The cited prior art fails to teach or suggest this feature of the claimed invention, as acknowledged by the Examiner (present Office Action; page 8, paragraph 3). Accordingly, claim 1, as amended, is believed to be patentable over the prior art of record. Therefore, favorable reconsideration and allowance of claim 1 is respectfully solicited.

With regard to claims 2-4, 9, 12 and 13, which depend from claim 1, Applicant asserts that these claims are also patentable by virtue of their dependency from amended claim 1, which is believed to be patentable for at least the reasons set forth above. Accordingly, favorable reconsideration and allowance of claims 2-4, 9, 12 and 13 are respectfully requested.

Claims 6 and 10 stand rejected under §103(a) as being unpatentable over one or both of the Miwa and Gomi references. Applicant asserts that these claims, which depend from amended claim 1, are also patentable by virtue of their dependency from claim 1, which is believed to be patentable for at least the reasons given above. Accordingly, favorable reconsideration and allowance of claims 6 and 10 are respectfully solicited.

Claims 16 and 17 have been added. Applicant submits that these claims, which depend from claim 1, are also patentable by virtue of their dependency from claim 1, which is believed to be patentable for at least the reasons given above. Accordingly, favorable consideration and allowance of claims 16 and 17 are respectfully requested.

device claim, not considered

For at least the foregoing reasons, Applicant believes that pending claims 1-13, 16 and 17 are in condition for allowance, and respectfully request withdrawal of the §102 and §103 rejections.

Attached hereto is a marked-up version of the changes made to the claims by the present Amendment. The attachment is captioned "Version with Markings to Show Changes Made."

Respectfully submitted,

Date: July 3, 2003

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Enclosure(s): Proposed Red-Lined Drawing Change to FIGS. 13 and 14 (2 sheets)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT

The abstract beginning at page 26, line 2, has been deleted and replaced with the following rewritten abstract:

Complementary bipolar transistors are fabricated on a semiconductor wafer by forming, on an upper surface of the semiconductor wafer, a first electrode corresponding to a first transistor, and a second electrode corresponding to a second transistor which is complementary to the first transistor. A first impurity is selectively introduced into the first and second electrodes. [Then, a] A third electrode corresponding to the first transistor [if] is formed, the third electrode being self-aligned with and electrically isolated from the first electrode, and a fourth electrode is formed corresponding to the second transistor, the fourth electrode being self-aligned with and electrically isolated from the second electrode. A second impurity is selectively introduced into the third and fourth electrodes. A first active region of the first transistor and a first active region of the second transistor are formed, whereby at least a portion of the first impurity associated with the first and second electrodes diffuses into the first active regions of the first and second transistors. Likewise, a second active region of the first transistor and a second active region of the second transistor are formed, whereby at least a portion of the second impurity associated with the third and fourth electrodes diffuses into the second active regions of the first and second transistors. A reduction in the number of fabrication steps and/or masks is thereby achieved which reduces an overall cost of fabricating complementary bipolar transistors.

IN THE CLAIMS

Claims 14 and 15 have been canceled without prejudice.

Claims 1-3, 5, 7, 8, 11 and 13 have been amended by rewriting same a follows:

1. (Amended) A method of fabricating complementary bipolar transistors on a semiconductor wafer, the method comprising the steps of:

forming a first electrode corresponding to a first transistor, and a second electrode corresponding to a second transistor which is complementary to the first transistor, the first and second electrodes being formed on an upper surface of the semiconductor wafer;

selectively introducing a first impurity into the first and second electrodes;

forming a third electrode corresponding to the first transistor, the third electrode being self-aligned with and electrically isolated from the first electrode, and forming a fourth electrode corresponding to the second transistor, the fourth electrode being self-aligned with and electrically isolated from the second electrode;

selectively introducing a second impurity into the third and fourth electrodes;

forming a first active region of the first transistor and a first active region of the second transistor, whereby at least a portion of the first impurity associated with the first and second electrodes diffuses into the first active regions of the first and second transistors; and

forming a second active region of the first transistor and a second active region of the second transistor, whereby at least a portion of the second impurity associated with the third and fourth electrodes diffuses into the second active regions of the first and second transistors;

wherein at least one of:

the step of forming the first and second electrodes further comprises rapid thermal annealing the semiconductor wafer for substantially removing residual oxide between the first polysilicon layer and the upper surface of the semiconductor wafer; and

the step of forming the third and fourth electrodes further comprises rapid thermal annealing the semiconductor wafer for substantially removing residual oxide between the second polysilicon layer and the upper surface of the semiconductor wafer.

2. (Amended) The method of claim 1, further comprising the step of:

forming a dielectric spacer on a vertical sidewall portion of each of at least the first and second electrodes, the dielectric spacers electrically isolating at least the first and second electrodes from an adjacent structure formed on [an] the upper surface of the semiconductor wafer.

3. (Amended) The method of claim 2, wherein the step of forming the [at least one] dielectric [spacer] spacers comprises the steps of:

performing at least one of depositing an oxide layer on the upper surface of the [substrate] semiconductor wafer and growing an oxide layer on [an] the upper surface of the semiconductor wafer; and

etching the [semiconductor wafer] oxide layer until the oxide layer on a horizontal portion of the semiconductor wafer is substantially removed and the oxide layer substantially remains on the sidewall portions of at least the first and second electrodes.

5. (Amended) [The method of claim 4,] A method of fabricating complementary bipolar transistors on a semiconductor wafer, the method comprising the steps of:

forming a first electrode corresponding to a first transistor, and a second electrode corresponding to a second transistor which is complementary to the first transistor, the first and second electrodes being formed on an upper surface of the semiconductor wafer;

selectively introducing a first impurity into the first and second electrodes;

forming a third electrode corresponding to the first transistor, the third electrode being self-aligned with and electrically isolated from the first electrode, and forming a fourth electrode corresponding to the second transistor, the fourth electrode being self-aligned with and electrically isolated from the second electrode;

selectively introducing a second impurity into the third and fourth electrodes;

forming a first active region of the first transistor and a first active region of the second transistor, whereby at least a portion of the first impurity associated with the first and second electrodes diffuses into the first active regions of the first and second transistors; and

forming a second active region of the first transistor and a second active region of the second transistor, whereby at least a portion of the second impurity associated with the third and fourth electrodes diffuses into the second active regions of the first and second transistors;

wherein the step of forming the first and second electrodes comprises the steps of:

forming a first polysilicon layer on the upper surface of the semiconductor wafer;

forming a hard mask layer on the first polysilicon layer;

selectively patterning the hard mask layer to define predetermined areas of the first polysilicon layer to be etched; and

etching away the predetermined areas of first polysilicon layer; and

wherein the step of forming the first and second electrodes further comprises rapid thermal annealing the semiconductor wafer for substantially removing residual oxide between the first polysilicon layer and the upper surface of the semiconductor wafer.

7. (Amended) [The method of claim 6,] A method of fabricating complementary bipolar transistors on a semiconductor wafer, the method comprising the steps of:

forming a first electrode corresponding to a first transistor, and a second electrode corresponding to a second transistor which is complementary to the first transistor, the first and second electrodes being formed on an upper surface of the semiconductor wafer;

selectively introducing a first impurity into the first and second electrodes;

forming a third electrode corresponding to the first transistor, the third electrode being self-aligned with and electrically isolated from the first electrode, and forming a fourth electrode

corresponding to the second transistor, the fourth electrode being self-aligned with and electrically isolated from the second electrode;

selectively introducing a second impurity into the third and fourth electrodes;

forming a first active region of the first transistor and a first active region of the second transistor, whereby at least a portion of the first impurity associated with the first and second electrodes diffuses into the first active regions of the first and second transistors; and

forming a second active region of the first transistor and a second active region of the second transistor, whereby at least a portion of the second impurity associated with the third and fourth electrodes diffuses into the second active regions of the first and second transistors;

wherein the step of forming the first and second electrodes comprises the steps of:

forming a first polysilicon layer on the upper surface of the semiconductor wafer;

forming a hard mask layer on the first polysilicon layer;

selectively patterning the hard mask layer to define predetermined areas of the first polysilicon layer to be etched; and

etching away the predetermined areas of first polysilicon layer;

wherein the step of forming the third and fourth electrodes comprises the steps of:

forming a second polysilicon layer on the upper surface of the semiconductor wafer;

forming a hard mask layer on the second polysilicon layer;

selectively patterning the hard mask layer to define predetermined areas of the second polysilicon layer to be etched; and

etching away the predetermined areas of the second polysilicon layer; and

wherein the step of forming the third and fourth electrodes further comprises rapid thermal annealing the semiconductor wafer for substantially removing residual oxide between the second polysilicon layer and an upper surface of the semiconductor wafer.

8. (Amended) [The method of claim 1,] A method of fabricating complementary bipolar transistors on a semiconductor wafer, the method comprising the steps of:

forming a first electrode corresponding to a first transistor, and a second electrode corresponding to a second transistor which is complementary to the first transistor, the first and second electrodes being formed on an upper surface of the semiconductor wafer;

selectively introducing a first impurity into the first and second electrodes;

forming a third electrode corresponding to the first transistor, the third electrode being self-aligned with and electrically isolated from the first electrode, and forming a fourth electrode corresponding to the second transistor, the fourth electrode being self-aligned with and electrically isolated from the second electrode;

selectively introducing a second impurity into the third and fourth electrodes;

forming a first active region of the first transistor and a first active region of the second transistor, whereby at least a portion of the first impurity associated with the first and second electrodes diffuses into the first active regions of the first and second transistors; and

forming a second active region of the first transistor and a second active region of the second transistor, whereby at least a portion of the second impurity associated with the third and fourth electrodes diffuses into the second active regions of the first and second transistors;

wherein the steps of forming the first, second, third and fourth electrodes comprises:

forming a first polysilicon layer on the upper surface of the semiconductor wafer;

forming a hard mask layer on the first polysilicon layer;

selectively patterning the hard mask layer to define predetermined areas of the first polysilicon layer to be etched;

etching away the predetermined areas of the first polysilicon layer to form the first and second electrodes;

forming dielectric spacers on vertical sidewall portions of each of the first and second electrodes;

forming a second polysilicon layer on the upper surface of the semiconductor wafer;

performing a blanket etch-back of the semiconductor wafer until at least a portion of each of the dielectric spacers on the sidewalls of the first and second electrodes is detected at [an] the upper surface of the semiconductor wafer;

selectively patterning the second polysilicon layer to define predetermined areas of the second polysilicon layer to be etched; and

etching away the predetermined areas of the second polysilicon layer to form the third and fourth electrodes.

11. (Amended) [The method of claim 1, further comprising the steps of:] A method of fabricating complementary bipolar transistors on a semiconductor wafer, the method comprising the steps of:

forming a first electrode corresponding to a first transistor, and a second electrode corresponding to a second transistor which is complementary to the first transistor, the first and second electrodes being formed on an upper surface of the semiconductor wafer;

selectively introducing a first impurity into the first and second electrodes;

forming a third electrode corresponding to the first transistor, the third electrode being self-aligned with and electrically isolated from the first electrode, and forming a fourth electrode corresponding to the second transistor, the fourth electrode being self-aligned with and electrically isolated from the second electrode;

selectively introducing a second impurity into the third and fourth electrodes;

forming a first active region of the first transistor and a first active region of the second transistor, whereby at least a portion of the first impurity associated with the first and second electrodes diffuses into the first active regions of the first and second transistors;

forming a second active region of the first transistor and a second active region of the second transistor, whereby at least a portion of the second impurity associated with the third and fourth electrodes diffuses into the second active regions of the first and second transistors;

forming a dielectric layer on the semiconductor wafer such that an upper surface of the semiconductor wafer is substantially planar;

forming a plurality of contact windows at predetermined areas in the dielectric layer;

depositing a conductive layer on the upper surface of the semiconductor wafer; and

selectively patterning the conductive layer to form a plurality of contacts, the contacts being electrically connected to respective electrodes associated with the complementary bipolar transistors.

13. (Amended) The method of claim 1, further comprising the step of:

performing a controlled rapid thermal anneal on the semiconductor wafer, whereby [predetermined] one or more electrical characteristics of the complementary bipolar transistors are set to a desired value.

Claims 16 and 17 have been added:

16. (New) A pair of complementary bipolar transistors formed according to the method of claim 1.

17. (New) An integrated circuit including at least one pair of complementary bipolar transistors, the at least one pair of complementary bipolar transistors formed according to the method of claim 1.

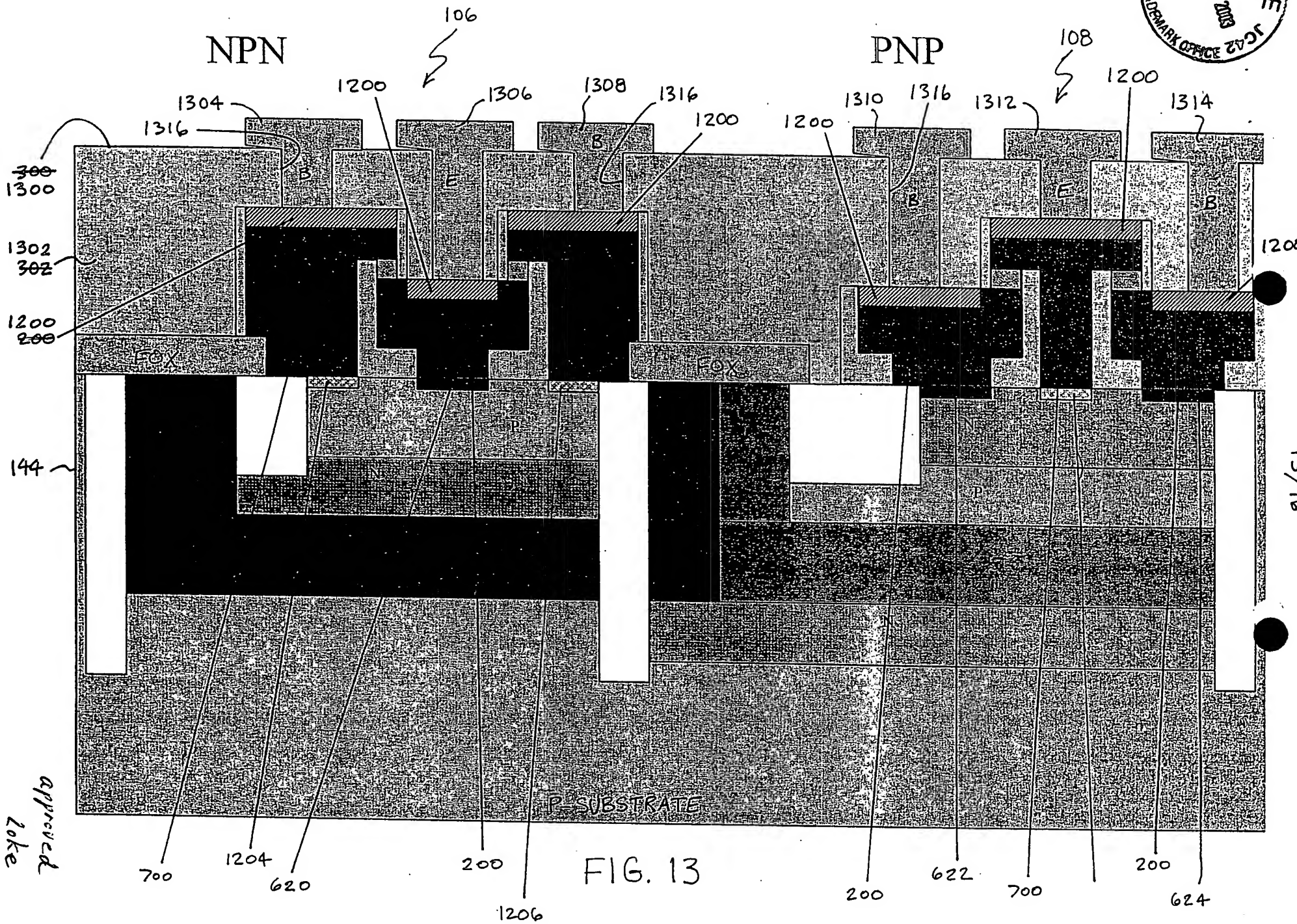

FIG. 13

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Case II

NPN

PNP

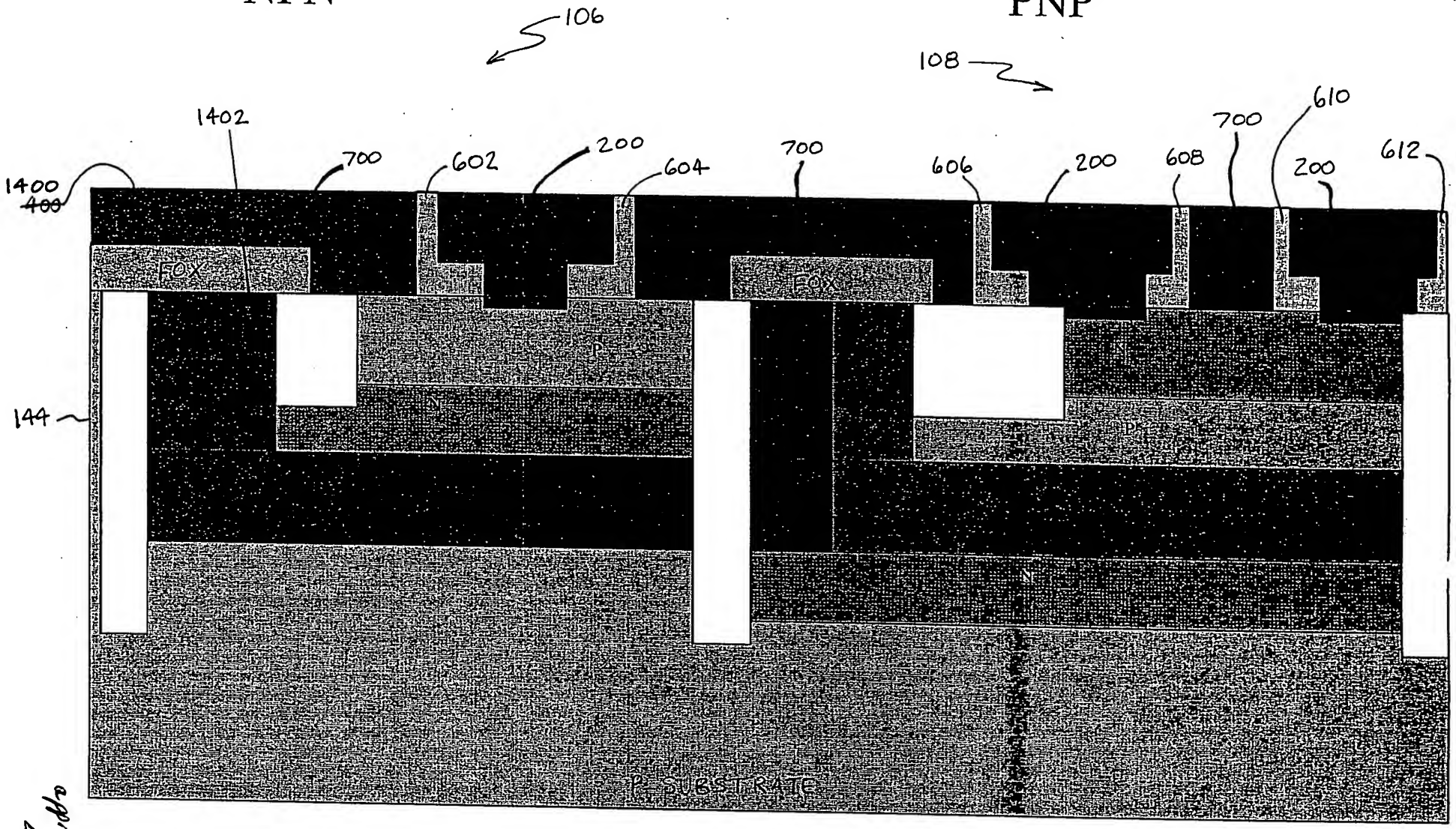

FIG. 14

approved
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